Mitigation of Functional Power Dissipation in Parasitic Scan Shift Test Buffers

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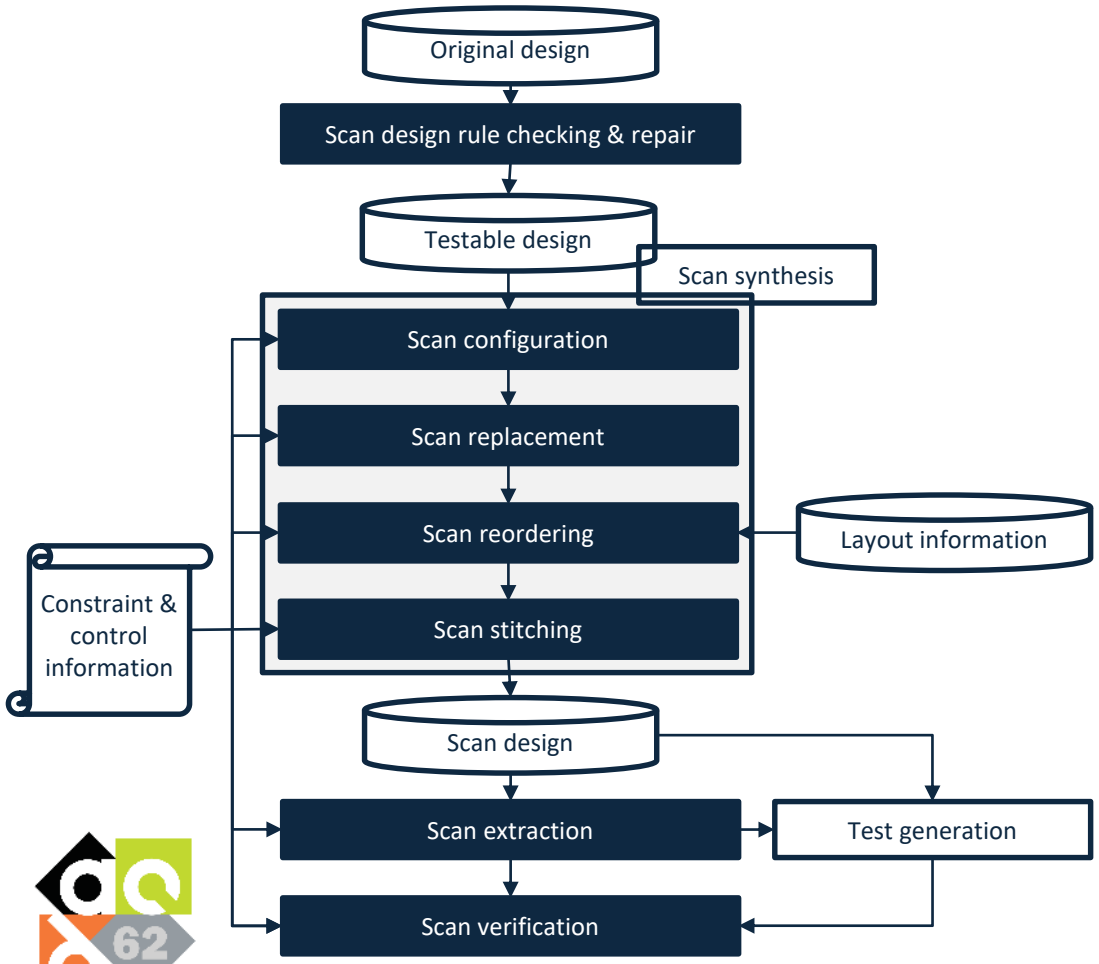
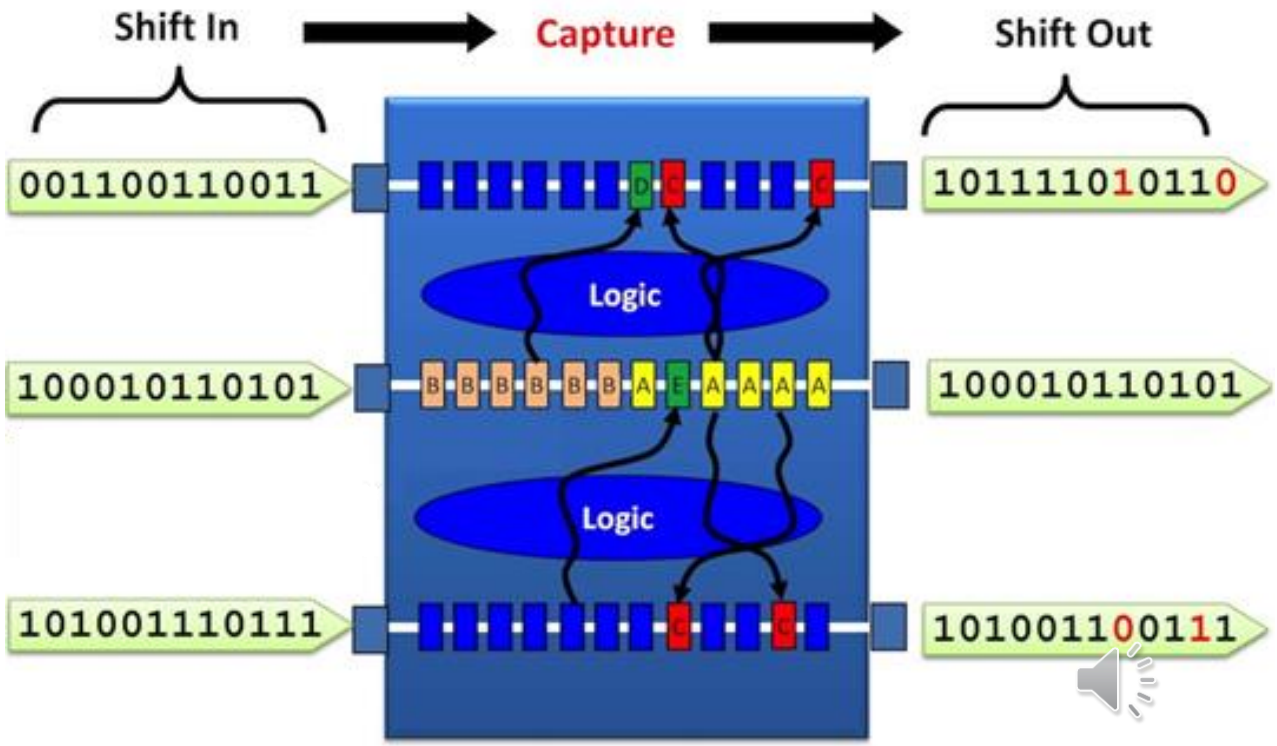
Digital scan-based DFT

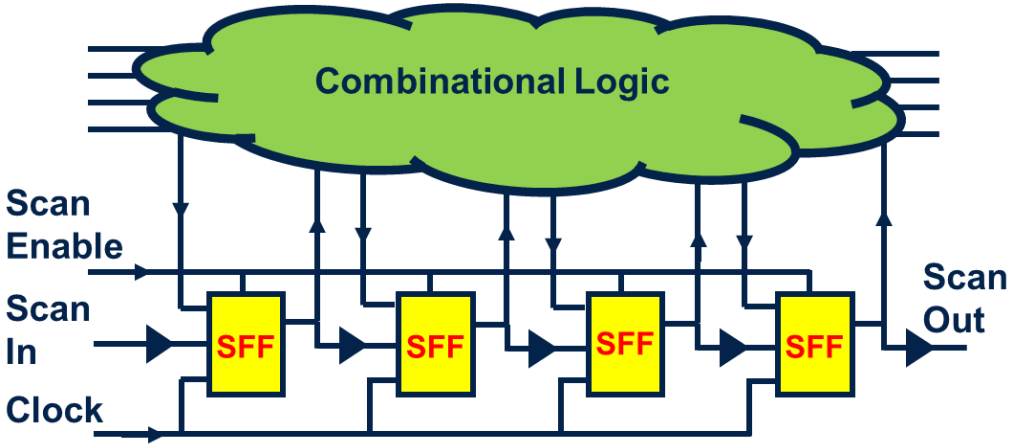
From Scan-Shift and Hold-Time violations to Hold-Time fixing buffers

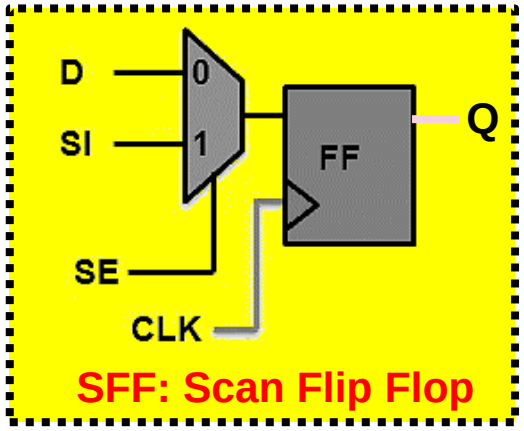




Motivation

Dynamic power savings in Functional mode

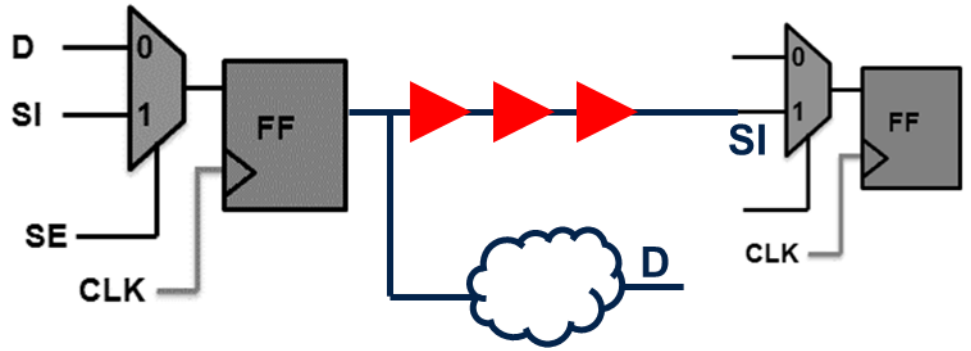




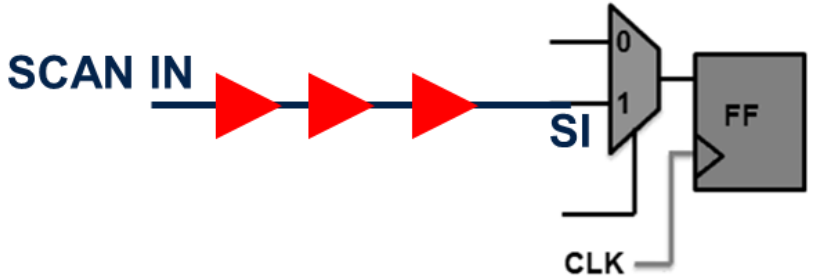
- **Buffers to fix hold** time violations in scan-test shift paths **switch in both functional & scan** modes
- These buffers stay connected to functional paths and shall **consume power for the lifetime of the chip.**
- The problem becomes worse in **multiclock domain designs**
- In functional mode, **power dissipation** of these buffers **is a waste**
- EDA tool ability to **identify these 'parasitic' buffers** should be leveraged to **isolate them in functional mode**

Scan Buffers in Functional Modes

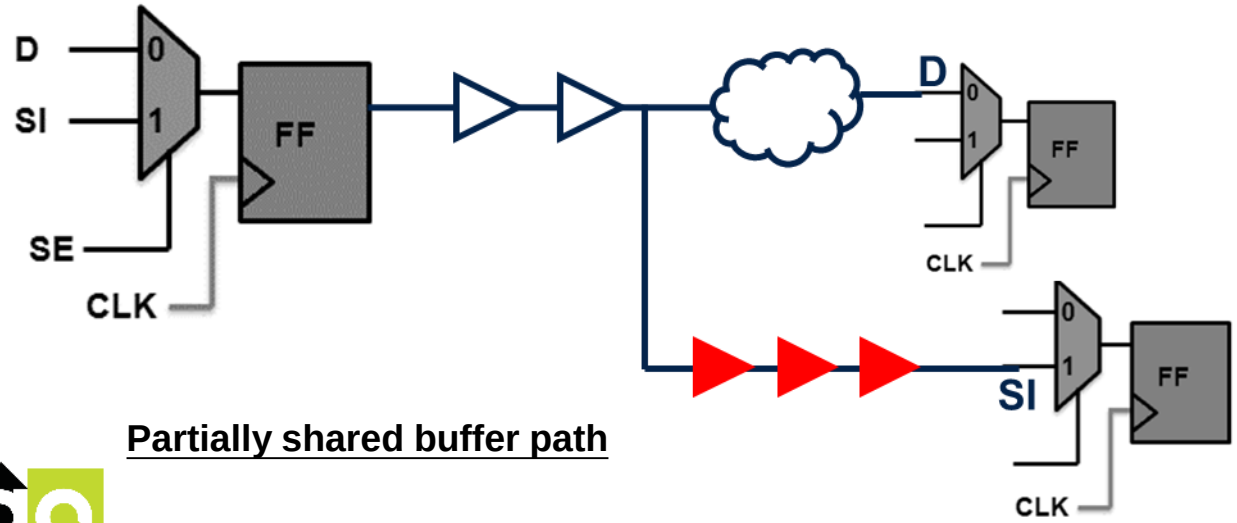
Hold-Time Fixing Buffers paths



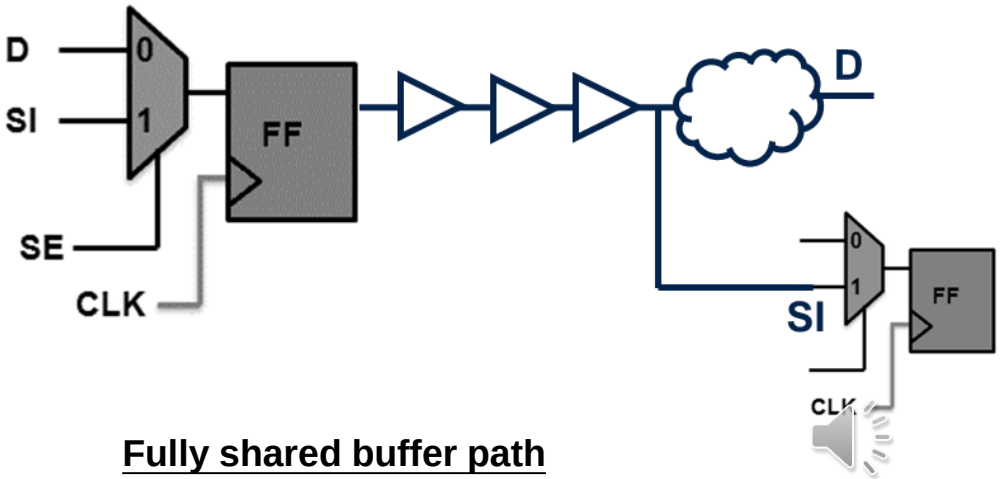
Dedicated buffer path



Primary scan-in



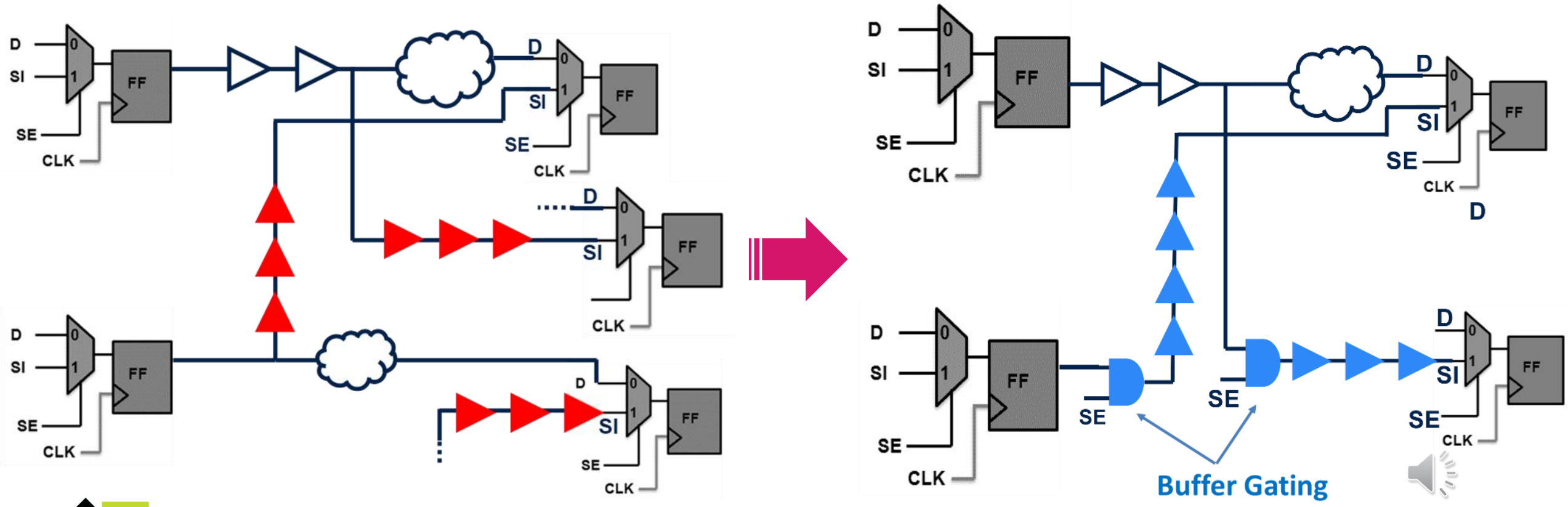
Partially shared buffer path



Fully shared buffer path

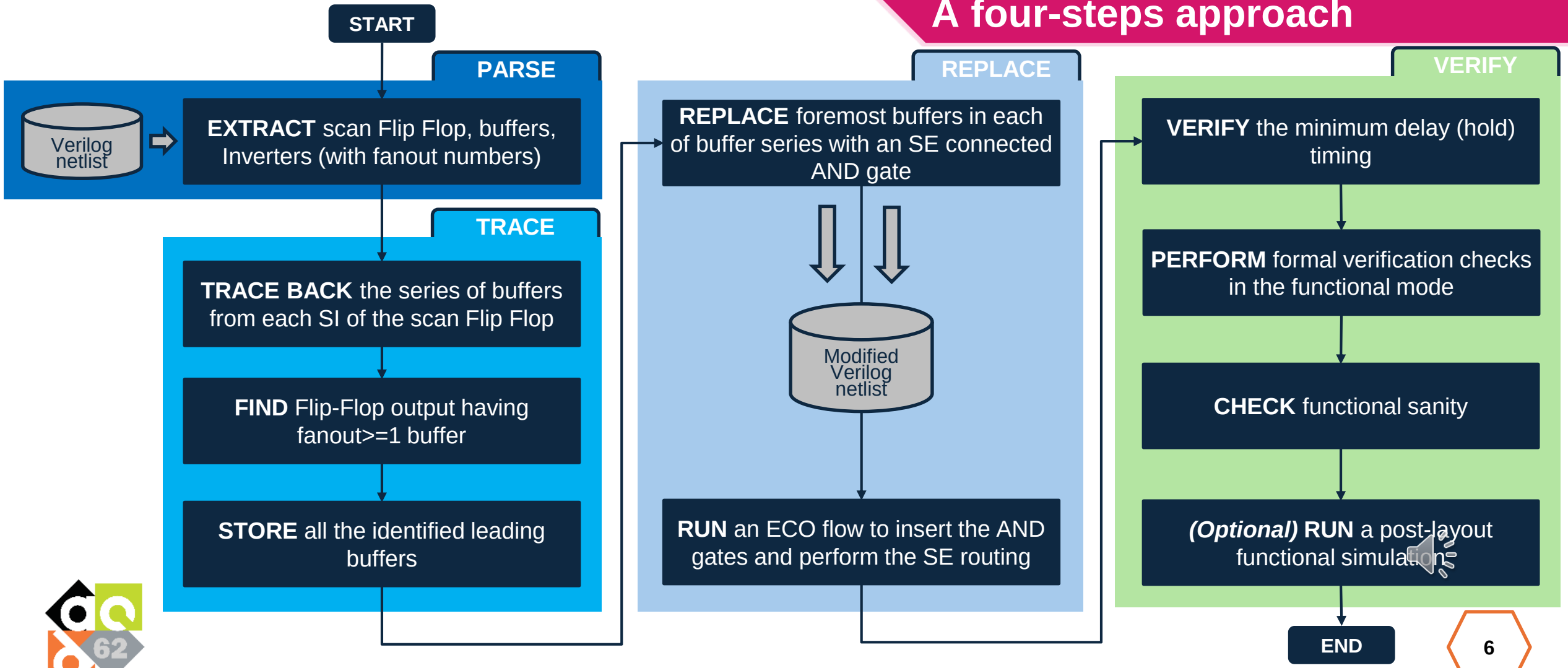
Main idea

Isolate dedicated buffers in functional mode

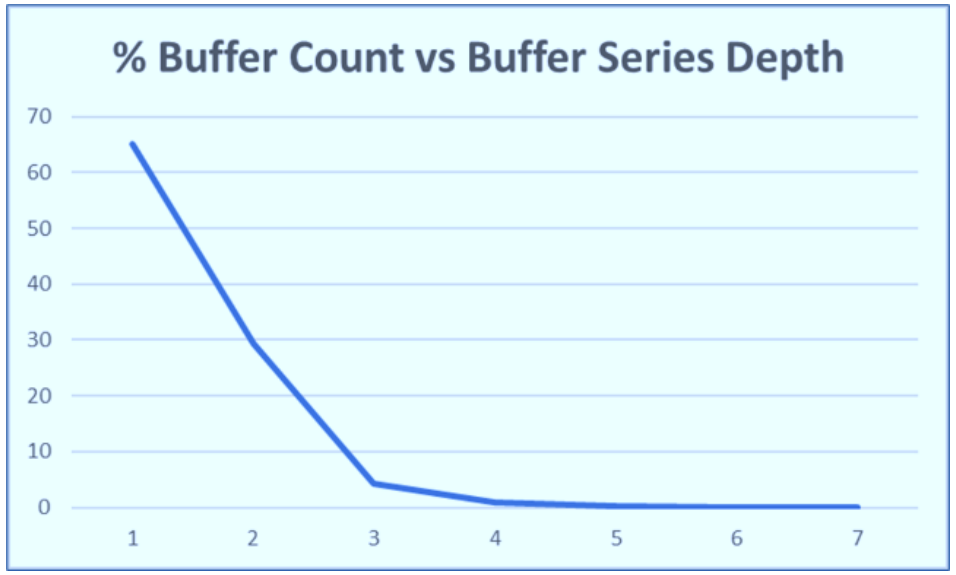


Proposed automation flow

A four-steps approach



Results



Design Type	Maximum functional frequency	Scannable registers count	Hold fix buffer count	Dynamic power saving
Filter Chain	2.4 GHz	3739	2799	**7.8 %**
CPU Cluster	800 MHz	332356	154359	**4.5 %**

Significant dynamic power savings

Trends in hold fix buffer usage specifically for scan shift mode

- At 65%, single buffers usage is maximum
- 25% two series connected buffers
- 5% three series connected buffers

Technique applied to diverse designs

- **8% savings** in a high-speed ΣΔ ADC decimation filter chain running @2.4GHz
- **4.5% savings** in an automotive CPU cluster with its core running @800 MHz

Takeaways

An effective technique & automation flow for reducing dynamic power

- Achieved **without any** design or implementation **trade-offs** (get for free!)
- **Power recovery** is moderate for large sized, medium frequency designs and **higher for smaller high frequency blocks**
- All **present and future digital circuits can easily adopt** the proposed buffer gating technique without any ramifications
- **Agnostic of the chip architecture**, design size, technology node
- An **implementation-based technique** that might be deployed w/o hampering design
- The proposed methodology can be implemented with **existing EDA tools** and w/o impacting the design cycle

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Power-aware DFT techniques

Saving power in Test Mode

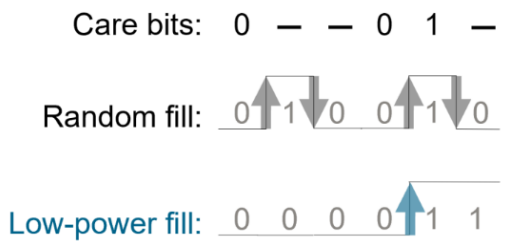

Fig. 1: Replicating care bits for low power shift

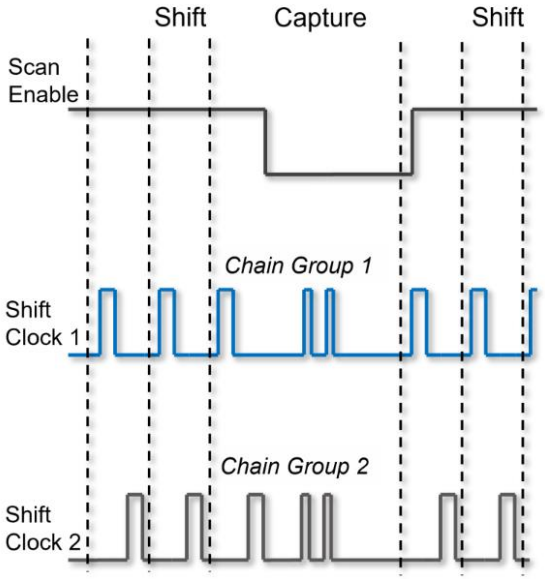

Fig. 2: Shift Clock 1 and Shift Clock 2 staggered during shift phase to reduce shift power

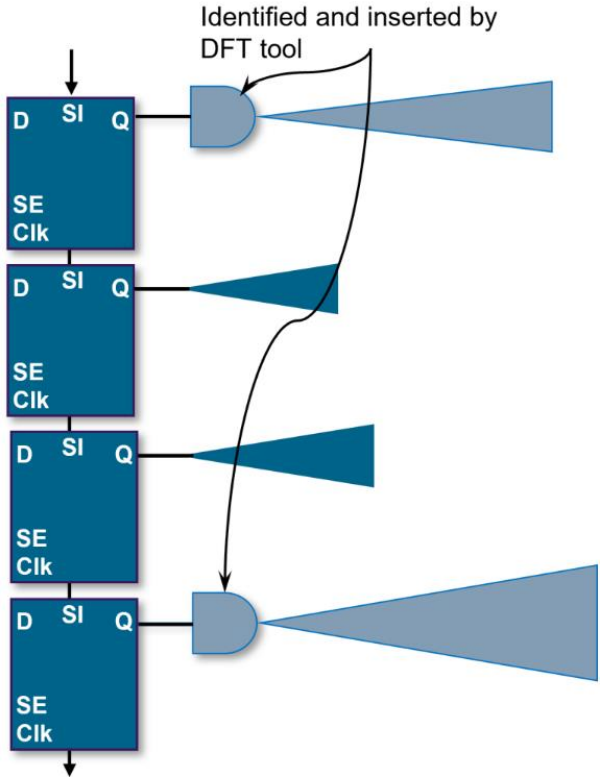

Fig. 3: Disabling activity of high fanout combinational logic to reduce power

Fig. 4: Low power shift using SPC chain in compression logic

functional power constraints must also be followed in the test domain by generating test patterns such that test power does not exceed the chip power budget.
This avoids potentially damaging the chip or triggering a false test pattern failure due to power supply droops, both causing unnecessary yield loss.
At the same time, the test patterns should be able to utilize the entire available power budget to maintain test quality and cost.
This is challenging because under-constraining test patterns would violate the power budget while over-constraining could result in pattern count inflation and/or lower test coverage

Ref: https://semiengineering.com/power-aware-test-addressing-power-challenges-in-dft-and-test/